	Title	Current OR	Current XRef
1	Overvoltage protection circuits that utilize capacitively bootstrapped variable voltages	361/56	361/111
2	Input gate protection circuit and method	361/56	361/111
3	Stress-follower circuit configuration	361/90	326/87; 327/381
4	Enhanced protection for input buffers of low-voltage flash memories	326/83	326/81
5	Adjustable trigger voltage circuit for sub-micrometer silicon IC ESD protection	361/56	361/111
6	Low skew, power sequence independent CMOS receiver device	327/333	327/62
7	Using thick-oxide CMOS devices to interface high voltage integrated circuits	327/319	326/80; 327/323; 327/333
8	I/O pad voltage protection circuit and method	361/111	327/310; 361/56
9	Stress-follower circuit configuration	361/90	326/87; 327/381
10	Pad driver	327/318	327/108; 327/309
11	High speed buffer circuit with improved noise immunity	326/83	326/119; 326/27
12	Stress-follower circuit configuration	361/56	326/83
13	Circuit and method for protecting input/output stage of a low voltage integrated circuit device from a failure of the internal power supply or in the power-up sequencing of power supplies	361/86	361/111; 361/91.5
14	Bus driver having noise removing circuit	326/26	326/27; 326/86; 326/90

	Title	Current OR	Current XRef
15	Using thick-oxide CMOS devices to interface high voltage integrated circuits	327/534	327/108; 327/110; 327/325; 361/56; 361/91.1
16	Overshoot/undershoot protection scheme for low voltage output buffer	327/389	326/27; 326/83; 327/391; 361/91.1; 361/91.5
17	Low voltage CMOS input buffer with undershoot/overshoot protection	326/83	326/121; 326/22; 326/31; 327/205
18	Overvoltage and electrostatic discharge protection for a receiver circuit	361/56	327/328; 361/91.5
19	Dynamic biasing for overshoot and undershoot protection circuits	327/534	326/27; 326/33; 326/34; 327/108; 327/309; 327/312; 327/537
20	Cascoded-MOS ESD protection circuits for mixed voltage chips	361/56	327/310; 361/111